Electronic Version
Stylesheet Version v1.1.1

Description

[SEMICONDUCTOR DEVICE AND FABRICATING METHOD THEREOF]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92119109, filed on July 14, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention relates to an integrated circuit and fabricating method thereof. More particularly, the present invention relates to a semiconductor device and method of fabricating the same.

[0004] Description of the Related Art

[0005] Typically, integrated circuit devices are interconnected via metal interconnects. The conventional method of fabricating metal interconnects includes forming a metal plug in a dielectric layer and then forming a metal line over a substrate to connect with the metal plug. Fig. 1 is a top view

showing the layout of conventional metal interconnects. As the level of integration for semiconductor devices continues to increase, the aspect ratio of contact openings must be reduced to avoid difficulties encountered while carrying out etching and material deposition. At present, the contact plug 20 in Fig. 1 has a critical dimension greater than the metal line 10 so that more metal lines 10 can be packed within the limited surface area of a chip.

[0006] With the contact plug 20 having a larger critical dimension, the alignment tolerance in the process of forming the contact opening is greatly reduced. Should an alignment error occur, a neighboring conductive structure such as the conductive layer of a gate structure may be exposed leading to a possible short circuit between a subsequently formed contact plug and the conductive structure.

[0007] Furthermore, with the critical dimension of the contact plug 20 greater than the metal line 10 and the pitch between neighboring metal line 10 reduced, the overlay tolerance in photolithographic processing of the metal lines 10 is relatively small. Any minor misalignment will likely lead to an unwanted electrical connection or short-circuit between a metal line 10 and a neighboring plug.

SUMMARY OF INVENTION

[0008] Accordingly, the present invention is to provide a semiconductor device and manufacturing method thereof for increasing overlay tolerance of metal interconnects.

[0009] This invention is to provide a semiconductor device and manufacturing method thereof for preventing a short circuit between a contact plug and a neighboring conductive structure.

[0010] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of manufacturing a semiconductor device. First, a conductive structure, spacers and a dielectric layer are formed over a substrate. Thereafter, a portion of the cap layer of the conductive structure, a portion of the spacer and a portion of the dielectric layer are removed by etching to form a funnel-shaped opening. The shoulder portion of the conductive layer within the conductive structure exposed by the funnel-shaped opening is removed to form a shoulder recess. A liner layer is formed on the sidewall of the funnel-shaped opening and then a bottom plug is formed in the funnel-shaped opening. Afterwards, another dielectric layer is formed over the substrate. A top plug is formed in the dielectric layer such that the top

plug and the bottom plug are electrically connected. Finally, a wire line is formed on the upper surface of the substrate.

[0011] In this invention, the contact/via plug is fabricated by combining two sections together, namely, a bottom plug and a top plug. With this setup, the aspect ratio of the contact/via opening in the process of forming the contact/via is very much reduced. Hence, the process of etching out contact/via openings and the deposition of conductive material into the opening thereafter is greatly simplified.

[0012] Because the top plug has a critical dimension smaller than the junction portion of the funnel shaped bottom plug, the alignment tolerance with respect to the bottom plug in the photolithographic process for forming the top plug opening is increased. Furthermore, with the top plug having a smaller critical dimension, the wire lines above the top plugs can have a larger alignment tolerance so that the probability of having a short circuit due to misalignment is lowered considerably.

[0013] In addition, the shoulder chamfer or shoulder recess in the conductive layer of the conductive structure permits the formation of a thicker liner layer in this area. There-

fore, the section between the bottom plug and the conductive layer, in particular, between the conductive layer and the shoulder section can have a thicker isolating liner layer for preventing plug/conductive layer short circuit.

[0014] This invention also provides a semiconductor device. The semiconductor device comprises a plurality of conductive structures, a plurality of bottom plugs, a plurality of top plugs, a plurality of wire lines, a liner layer and a dielectric layer. The conductive structures are formed over a substrate. The bottom plugs have a funnel shape. Furthermore, the bottom plugs are positioned between neighboring conductive structures and are electrically connected to the substrate. The liner layer is set up between the neighboring conductive structures and the bottom plug. The top plug is set up over the bottom plug. The junction between the bottom plug and the top plug has a critical dimension greater than the top plug. The wire lines are electrically connected to the respective top lugs. The dielectric layer is set up between the conductive structures, between the bottom plugs, between the top plugs and between the wire lines.

[0015] It is to be understood that both the foregoing general description and the following detailed description are exem-

plary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0016] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0017] Fig. 1 is a top view showing the layout of conventional metal interconnects.

[0018] Figs. 2A through 2F are schematic cross-sectional views showing the progression of steps for fabricating metal interconnects according to one preferred embodiment of this invention.

[0019] Fig. 3 is a top view of Fig. 2F.

Detailed Description

[0020] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like

parts.

[0021] Figs. 2A through 2F are schematic cross-sectional views showing the progression of steps for fabricating metal interconnects according to one preferred embodiment of this invention. As shown in Fig. 2A, a plurality of conductive structures 210 is formed over a substrate 200. Each conductive structure 210 at least comprises a conductive layer 206 and a cap layer 208. The conductive layer 206 further comprises a polysilicon layer 202 and a metal silicide layer 204, for example. The cap layer 208 is a silicon nitride layer, for example. Thereafter, spacers 212 are formed on the sidewalls of the conductive structures 210. The spacers 212 are silicon nitride layers formed by performing a chemical vapor deposition operation, for example. A dielectric layer 214 is formed over the substrate 100. The dielectric layer 214 is formed, for example, by depositing dielectric material over the cap layer 208 and into the space between the spacers on the conductive structures 210. This is followed by performing a chemical-mechanical polishing to remove the dielectric material above the cap layer 208. The dielectric layer 214 is fabricated using silicon oxide or borophosphosilicate glass (BPSG), for example.

[0022] As shown in Fig. 2B, a photoresist layer 216 is formed over the substrate 200. The photoresist layer 216 has an opening 218 that exposes the dielectric layer 214 between two neighboring conductive structures 210. Using the photoresist layer 216 as an etching mask, an anisotropic etching operation is carried out using an etchant having a high selectivity ratio between the dielectric layer 214 and the cap layer 208. Ultimately, the exposed dielectric layer 214 and a portion of the cap layer 212 and the spacers 212 are removed so that the shoulder section such as the metal silicide layer 204 of the conductive layer 206 is exposed. Because the etchant has a high etching selectivity ratio between the dielectric layer 214 and the cap layer 208/the spacers 212, a low etching rate for the cap layer 208 and the spacers 212 but a high etching rate for the dielectric layer 214, the opening 222 has a funnel shape after the etching operation.

[0023] As shown in Fig. 2C, the photoresist layer 215 is removed. A portion of the exposed conductive layer 206, that is, the shoulder portion of the metal silicide layer 204 is removed so that a shoulder chamfer or a shoulder recess 224 is formed. Thereafter, a liner material layer 226 is formed over the substrate 200 to cover the dielectric layer 214,

the cap layer 208 and the sidewall and bottom section of the funnel-shaped opening 222. The liner material layer 226 is fabricated using an insulating material such as silicon nitride or silicon oxide. The liner material layer 226 is formed, for example, by performing a chemical vapor deposition. Preferably, the liner material layer 226 is fabricated using a material that differs from a subsequently formed dielectric layer 230.

[0024] As shown in Fig. 2D, an anisotropic back etching is carried out to remove the liner material layer 228 over the dielectric layer 214 and the cap layer 208 and at the bottom of the funnel-shaped opening 222. The liner material layer 226a on the sidewalls of the funnel-shaped opening 222 is retained to serve as a liner layer. Since the conductive layer 206 has a shoulder chamfer or a shoulder recess 224, the liner layer 226a at the shoulder section of the conductive layer 206 is the thickest. Thereafter, a conductive layer 228 is formed over the substrate to cover the dielectric layer 214 and the conductive structure 210 and fill the funnel-shaped opening 222. The conductive layer 228 is fabricated using a metal material including tungsten or doped polysilicon, for example.

[0025] As shown in Fig. 2E, a chemical-mechanical polishing op-

eration is performed to remove the conductive layer 228 above the dielectric layer 214 and the conductive structure 210. Hence, a conductive layer 228a is retained within the funnel-shaped opening 333 to form a bottom plug. Thereafter, the dielectric layer 230 is formed over the substrate 200. The dielectric layer 230 has an opening 232 that exposes a portion of the bottom plug 228a. The opening 232 has a critical dimension smaller than the open end of the funnel-shaped opening 222. The dielectric layer 230 is a silicon oxide layer formed, for example, by performing a chemical vapor deposition. In general, the liner layer 226a is fabricated using a material that differs from the dielectric layer 230. Thus, even if there is some misalignment when the opening 232 is formed via a photolithographic process, the liner layer 226a may serve as an etching stop layer to prevent any over-etching in processing the dielectric layer 230.

[0026] As shown in Fig. 2F, another conductive layer is formed over the substrate 200 to cover the dielectric layer 230 and fill the opening 232. The conductive layer inside the opening 232 forms a top plug 234b. The conductive layer is fabricated using a metal material including, tungsten or doped polysilicon layer, for example. Thereafter, pho-

tolithographic and etching processes are carried out to pattern the conductive layer and form a plurality of wire lines 234a.

[0027] Fig. 2F is a schematic cross-sectional view of a semiconductor device structure according to a preferred embodiment of this invention. Fig. 3 is a top view of Fig. 2F. As shown in Figs. 2F and 3, the semiconductor device comprises a plurality of conductive structures 210, a plurality of bottom plugs 228a, a plurality of top plugs 234b, a plurality of wire lines 234a, a liner layer 226a and a pair of dielectric layers 214 and 230. The conductive structures 210 are formed over a substrate 200. The bottom plugs 228a is a solid block with a funnel shape. The bottom plugs 228 are positioned between neighboring conductive structures 210 and electrically connected to the substrate 200. The liner layer 226a is set up between neighboring conductive structures 210 and the bottom plugs 228a. The top plugs 234b, which are solid blocks with a cylindrical shape, are set up over the respective bottom plugs 228a. The junction portion of the bottom plug 228a connected to the top plug 234b has a critical dimension greater than the top plug 234b. The wire lines 234a are electrically connected to respective top plugs 234b. The

dielectric layer 214 is set up between the conductive structures 210 and between the bottom plugs 228a. The dielectric layer 230 is set up between the top plugs 234b and the wire lines 234a.

[0028] When this invention is applied to fabricate a memory device, the conductive structures 210 are gate structures that comprises a gate dielectric layer (not shown), a polysilicon layer 202, a metal silicide layer 204 and a cap layer 212. In this case, the wire lines 234a are bit lines and the top plug 234b and the bottom plug 228a together constitute a bit line contact.

[0029] In this invention, the contact/via plug is formed by combining two plug sections together, namely, a bottom plug 228a and a top plug 234b. With this setup, the aspect ratio of the contact/via opening in the process of forming the contact/via is reduced. Hence, the process of etching out contact/via openings and the deposition of conductive material into the opening thereafter is very much simplified. Note also that an anisotropic etching process is performed to remove a portion of the dielectric layer 214, the cap layer 208 and the spacers 212 and form a funnel-shaped opening 222. Since the funnel-shaped opening 222 has a critical dimension larger than the opening 232,

the photolithographic process for forming the opening 232 in the dielectric layer 230 can have a higher alignment tolerance with respect to the bottom plug 228a. Furthermore, with the opening 232 having a smaller critical dimension, the wire lines 234a above the top plugs 234b can have a larger alignment tolerance so that the probability of having a short circuit due to misalignment is lowered considerably.

[0030] In addition, the shoulder chamfer or shoulder recess 224 in the conductive layer 206 of the conductive structure 210 permits the formation of a thicker liner layer 226a in this area. Thus, the section between the bottom plug 228a and the conductive layer 206, in particular, between the conductive layer 206 and the shoulder section can have a thicker isolating liner layer 226a for preventing plug/conductive layer short circuit.

[0031] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.